REMARKS

Entry of this Amendment is proper because it narrows the issues on appeal and does not require further search by the Examiner.

Claims 3-17 are all the claims presently pending in the application. Claims 3-4, 6, 8 and 14 have been amended to more particularly define the invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claim 14 stands rejected under 35 U.S.C. § 112, first paragraph. Claims 8-10 and 16 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Iwata, et al. (U.S. Patent No. 5,880,500). Claims 3-7, 11-13, 15 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwata, et al.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (e.g., as claimed in claim 3) is directed to a method for manufacturing a semiconductor device (e.g., an n-type metal oxide semiconductor field effect transistor (NMOSFET)).

The method includes implanting arsenic ions in a semiconductor substrate at a first acceleration energy level which suppresses a reverse channel effect to form arsenic ion implanted regions, implanting phosphorous ions in the arsenic ion implanted regions, following the arsenic ion implanting, at a second acceleration energy level lower than the first acceleration energy level, so as to form a concentration peak of the phosphorous ions located in the arsenic ion implanted regions, an ion-implanted region of the phosphorous ion extending an ion-implanted region of the arsenic ion and performing a heat treatment to activate the arsenic ions and the phosphorous ions in the ion-implanted regions to form source/drain regions and buffer regions which include phosphorous ions and extend beyond the source/drain regions.

Conventional methods of forming a source/drain regions in a semiconductor device (e.g., an NMOSFET) include implanting arsenic at an acceleration energy of about 50 keV in the source/drain region. However, as channel length and source/drain regions have become smaller, a reverse short channel effect has been realized in which the threshold voltage fluctuates largely for with a change in the length of the gate. Further, if the acceleration energy of implantation is lowered to eliminate this reverse short channel effect, an undesirable increase in leakage current occurs.

The claimed method, on the other hand, implants phosphorous in the arsenic implanted regions to form a buffer region that extends beyond (e.g., below) the source/drain region. This allows the claimed invention to suppress a reverse short channel effect without increasing the p-n junction leakage current (Application at page 14, lines 13-22).

II. THE 35 USC §112, FIRST PARAGRAPH REJECTION

The Examiner alleges that claim 14 is not enabled by the specification. Applicant notes, however, that this claim has been amended to address the Examiner's concerns. Therefore, Applicant respectfully submits that this claim is adequately enabled by the specification.

Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. THE IWATA REFERENCE

The Examiner alleges that Iwata teaches the claimed invention of claims 8-10 and 16, and makes obvious the invention of claims 3-7, 11-13, 15 and 17. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Iwata.

Iwata discloses a method of forming a semiconductor device in which phosphorous is implanted in a silicon substrate to form a first impurity diffusion region, and arsenic is later implanted to form a second impurity diffusion region (Iwata at Figure 1; col. 10, line 57-col. 11, line 15). Specifically, Iwata discloses a method in which first impurity regions 105 are formed by implanting phosphorous ions at an acceleration energy of 10-30 keV (Iwata at col. 11, lines 1-15). Thereafter, the impurities are activated at 850 to 900 °C (Iwata at col. 11,

lines 59-64). Thereafter, third impurity regions 108 are formed by implanting arsenic ions at 20-40 keV (Iwata at col. 12, lines 34-40).

However, Applicant respectfully submits that Iwata clearly does not teach or suggest a method of forming a semiconductor device which includes *"implanting phosphorous ions in the arsenic ion implanted regions, following the arsenic ion implanting step"* as recited in claims 3 and as similarly recited in claim 8. As noted above, this feature is important because it allows the claimed method to suppress a reverse short channel effect without increasing the p-n junction leakage current (Application at page 14, lines 13-22).

The Application explains that the inventors of the claimed invention found that when phosphorous ions are implanted into an arsenic implanted region, a subsequent heat treatment causes the phosphorous ions to diffuse shallower than phosphorous ions implanted without a previous arsenic implantation (Application at page 11, lines 1-5). This is because the point defects generated by the phosphorous ion implantation are absorbed by the amorphous silicon layer generated by the arsenic ion implantation, so that the diffusion of the phosphorous ion assisted by the point defects is weakened (Application at page 11, lines 6-10).

Therefore, the inventors have discovered that by implanting phosphorous after implanting arsenic, the distance between the amorphous silicon/ monocrystalline silicon interface and a p-n junction interface can be increased. This allows the arsenic implantation energy to be reduced to eliminate the reverse short channel effect, without causing the p-n junction leakage current to increase (Application at page 10, lines 15-22).

Clearly, Iwata does not teach or suggest these novel features. Indeed, as noted above, Iwata does not even recognize one of the discoveries made by the inventors of the claimed invention, namely that when phosphorous ions are implanted into an arsenic implanted region, a subsequent heat treatment causes the phosphorous ions to diffuse shallower than phosphorous ions implanted without a previous arsenic implantation.

The Examiner concedes that Iwata does not teach or suggest implanting phosphorous ions in the arsenic ion implanted regions, following the arsenic ion implanting. However, he alleges that it would have been obvious to modify the Iwata method so as to implant the arsenic ions, then implant the phosphorous ions in the arsenic ion implanted region. Specifically, the Examiner alleges that this is merely selecting the order of forming.

The Examiner surprising believes that it makes no difference whether the arsenic ions or the phosphorous ions are implanted first. However, this is clearly contradicted by the Application. Indeed, the Examiner apparently is ignoring important large portions of the Application which clearly explain in great detail the importance of forming the arsenic ion implanted regions.

Indeed, as noted above, the Application explains that when phosphorous ions are implanted into an arsenic implanted region, a subsequent heat treatment causes the phosphorous ions to diffuse shallower than phosphorous ions implanted without a previous arsenic implantation (Application at page 11, lines 1-5). This is because the point defects generated by the phosphorous ion implantation are absorbed by the amorphous silicon layer generated by the arsenic ion implantation, so that the diffusion of the phosphorous ion assisted by the point defects is weakened (Application at page 11, lines 6-10).

In other words, contrary to the Examiner's allegations, the order of the implantation is important. This is clearly set forth in the Application.

Applicant respectfully submits that the Examiner cannot merely ignore the clear statements of fact presented in the Application in a desperate attempt to reject the claims in this case. Further, if the Examiner disagrees with the statements made in the Application (i.e., if he believes that the statements are erroneous), then the Examiner must so inform the Applicant so that the Applicant may respond accordingly.

Further, Applicant notes that this is not a case where the Application merely sets forth an order of processing steps. Instead, in this case, the Application specifically explains why it is important for the phosphorous ions to be implanted in the arsenic ion implanted regions. Therefore, the Examiner must address this in his rejection by providing some documentation which contradicts these statements in the Application. Otherwise, the Examiner must allow the case.

Moreover, the Examiner fails to recognize that Iwata requires that the third impurity region 108 (e.g., a arsenic implanted region) is formed after the first impurity region 105 (e.g., a phosphorous implanted region) (Iwata at col. 23, lines 1-24). That is, Iwata requires that the first impurity (e.g., phosphorous) is implanted before forming the metal silicide film, whereas the third impurity (e.g., arsenic) is implanted after the metal silicide film is formed.

(Iwata at col. 23, lines 1-5). Iwata explains that "since the third impurity is introduced after the silicidation reaction, a high concentrated impurity diffusion region can be made without interfering with the silicidation reaction" (Iwata at col. 23, lines 16-18).

Therefore, it is clearly unreasonable to suggest that one of ordinary skill in the art would have modified the process of Iwata, to form the claimed invention.

Therefore, Applicant submits that Iwata does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 3-17, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 7/21/03

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment was filed by facsimile with the United States Patent and Trademark Office, Examiner Quang D. Vu, Group Art Unit # 2811 at fax number (703) 872-9319, this 21st day of July, 2003.

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